RESEARCH ARTICLE OPEN ACCESS

Design Of Digital Configurable Error Free Frequency Detector Using Strobe Signal.

Sayannika Banik, Mrs. J.K Kasthuri Bha
M. tech, VLSI Design SRM University, kattankulathur campus Chennai, Tamilnadu, India
Asst. Professor, Dept. of ECE SRM University, kattankulathur campus Chennai, Tamilnadu, India

Abstract
This paper presents a glitch free module using strobe signal which overcomes the limitation of delay mismatch in a wide range of applications. The proposed strobe signal logic can control the occurrence of glitch at both the rising edge and falling edge of the circuit. The theoretical demonstration of the glitch free operation of the proposed strobe signal module is also derived in the paper. The previously proposed digitally controlled delay lines (DCDL) has been compared to this technology. Simulation results show the correctness of the module with no delay mismatch with respect to the previously proposed DCDL. As an example application, the strobe signal logic is used in configurable error free frequency detector (a frequency counter) which can control the occurrence of glitch during the sudden modulation of the frequency. The employ of the proposed strobe signal can hold the operation of the gate for a specific time until the other gate completes its operation so that there is no delay mismatch.

Keywords—Digitally controlled delay lines(DCDL), Integral non linearity(INL),strobe signal, configurable error free frequency detector.

I. INTRODUCTION

This paper basically deals with the Glitching problem in integrated circuits. Glitch is an electrical pulse of short duration which is formed due to a fault in the circuit or design error. It can also be defined as an unnecessary signal transitions that do not have any functionality. Nowadays reducing power dissipitation is a critical topic. Low power, high speed, minimum area usage with simpler layout design in digital circuits continues to get more attention in consideration of product manufacturing. Previously many approaches were taken to reduce glitch by designing a DCDL. Glitching is a common design problem for DCDL circuits. The common application DCDL's is to process clock signals, therefore glitch free operation is mandatory. The historical approach to design a DCDl's [3] is by using a delay cells chain and a MUX to select the desired cell output. In this approach the MUX delay increases with the increase of the number of cells. But in the next approach of designing the tree based MUX topology the large delay is reduced. However this results in irregular structure and complicated layout design and also increases nonlinearity of the circuit. The further approach leads to a DCDL topology which is used in [4], this is designed using delay cells chain and each cell is constructed by using NAND gates but it has disadvantage as the input capacitance increases linearly with the number of cell and thus re introduces tradeoff. In [5] the DCDL is constructed by using a set of equal delay elements, where the multiplexer of previous DCDL structures are used in all cells. In this way the delay is used and the circuit becomes independent of the number of cells. The similar approach is carried out in [6] where it again uses the structure of delay elements but here each element is constructed by using three-state inverters(TINV) , but the pull up network of a TINV requires two series devices whereas NAND gate uses a single device thus it will have higher resolution than the NAND based DCDL's. In the next approach a cascaded structure of equal delay elements are used which is constructed using an inverter and an inverting multiplexer. This structure provides higher resolution than all the previous methods but due to different delays of the inverter and multiplexer it results in delay mismatch between odd and even control codes. Many approaches are seen to avoid Glitching in mux-based DCDL. In some topologies Glitching is avoided by using thermometer codes for control bits in the circuit which is composed of four NAND gates where the delay of the circuit is controlled by control bits Si. It adds an advantage as the Glitching is overcome but it is time consuming as this encoding passes through three states like pass state, turn state, post turn state. Glitching is avoided in this method if one control bit is delayed with respect to the other but this condition is not sufficient to avoid glitches as output glitches are present with stable input signal. In the recent approach a NAND based

DCDL was constructed which uses two sets of control bits S_i and T_i. But it provides a disadvantage as it requires three step switching mechanism of DCDL and is time consuming. Later on the approach was modified by using two step switching topology but it complicates the layout design as it uses a structure of equal delay elements each consisting of six nand gates. The drawback of this approach is its large complexity as for each generation of control bit the other has to pass through a series of three nand gates which will consume more time. The further modifications are done by using the clock tree structure and double clock functionality but these structures consume more area and are hard to design. Thus in this paper we present the design and experimental evaluation of the (STROBE).This logic circuit reduces area with low layout complexity and the control signal can be used it any platform and also it reduces the further chances for glitches to appear.

II. PREVIOUSLY PROPOSED NAND-BASED DCDL AND CONTROL BITS DRIVING CIRCUITS.

A. NAND Based DCDL using two control bits

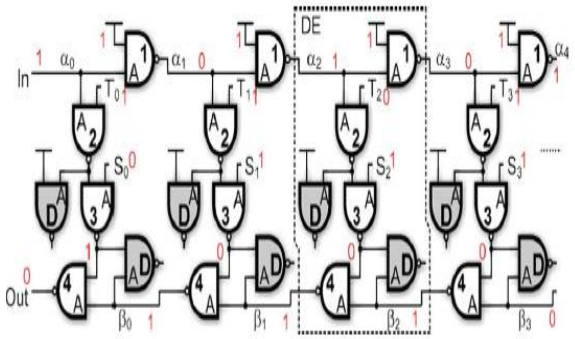

Fig.1.(a) Glitching problem of NAND based DCDL.

Fig. 1 shows NAND based DCDL, where the circuit comprises of series of equal delay elements each composed of six NAND gates. "A" in the figure denotes fast inputs of each NAND gate. "D" in the figure represents dummy cells added for load balancing. The delay of the circuit is controlled through two control bits S_i and T_i. The S_i bits encode the control code c by using thermometric code: $S_i = 0$ for $i < c$ and $S_i = 1$ for $i > c$. According to the control bits the delay element can be in any one of the three states (pass state, turn state, post turn state). The delay element with $i < c$ are in pass state where ($S_i = 0$ and $T_i = 1$), which leads to NAND "3" output equal to 1 and NAND "4" allows signal propagation in the lower NAND gates. When the delay element with $i = c$ is in turn state ($S_i = T_i = 1$), then the upper input of the delay element is passed to the output of NAND "3". Next delay element ($i = c + 1$) is in post turn state ($S_i = 1$, $T_i = 0$) where the output of the NAND "4" is stuck at 1. T logic state of α_i and β_i depends on the input. The circuit uses six NAND gates which consumes more area and thus makes the working slow. Thus the following section shows how the glitch is removed using two step mechanism.

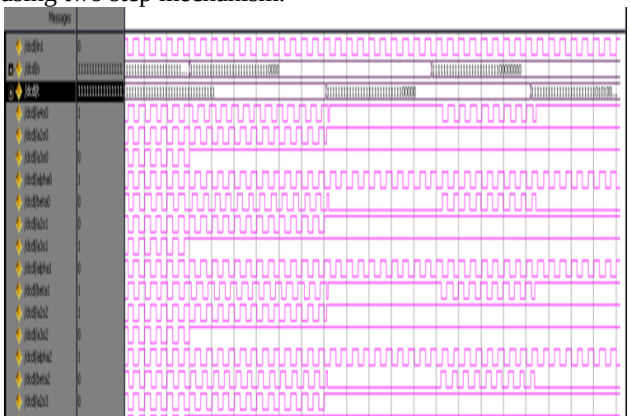

Fig. 1 (b) simulations highlighting glitches by using NAND based DCDL.

B. NAND Based DCDL using control bis driving circuits.

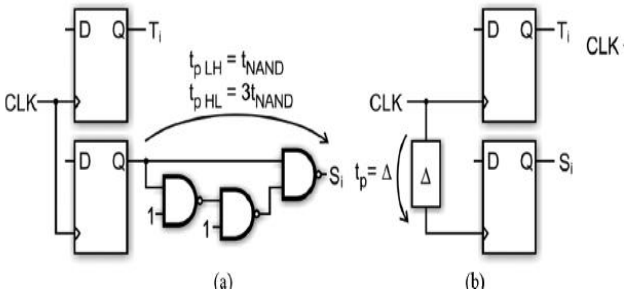

Fig.2. Driving circuits for control bits. (a) Si signal delayed with different LH/HL delays by using NAND based circuit. (b)Si signal delayed using clock tree delay.

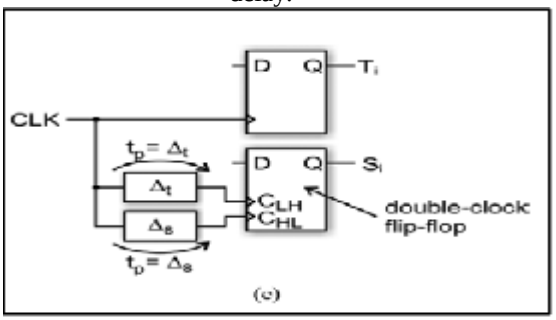

Fig.2. (c) Si delayed with different LH/HL delays by using clock tree delay and double clock flip flop.

The three step switching mechanism has been modified by using two step switching mechanism. Fig 2(a) shows three driving circuits that can be used to generate the control bits of proposed DCDL. According to the earlier concept to reduce glitch, the Si signals have to be delayed with respect to T_i signals. T_i signal is generated as the output of the flip flop and each Si signal is obtained by using a flip flop and a NAND based circuit.

Fig 2(b) shows an enhanced circuit compared to the previous, where Si signals are delayed by delaying the clock signal of the flip flop. The clock signal delay can be obtained by designing a clock tree. Fig 2(c) employs a flip flop using two different clock signals. C_{LH} captures the high logic state of D input whereas C_{HL} captures the low logic state of D input. But the major disadvantages follows as it consumes large area and complex design, moreover flip flops are prone to produce glitches and every time a glitch free topology has to be used in order to remove glitch. The major disadvantages of the previously proposed structure is its large area and layout complexity, moreover the code is not reusable for all the other circuits using the control bits. Due to this complex circuit and large area it will consume more power and the chances for the occurrence of glitch are even more, so in order to not only reduce the glitch but also creating a platform so that glitches will never occur in future we use strobe control logic.

III. PROPOSED STROBE SIGNAL MODULE

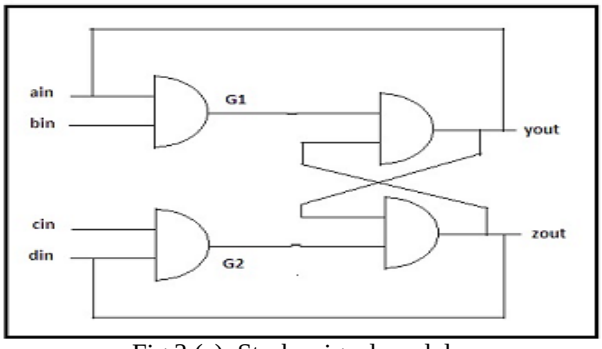

Fig.3 (a). Strobe signal module

We present the design and experimental evaluation of STROBE. Strobe is basically a control signal, which can hold the operation of a gate for a specific time period, so that there is no delay mismatch. Strobe can control the occurrence of the glitch at both the rising edge and the falling edge of the circuit. In the circuit shown when the strobe signal is 1, it will trigger the gate1 and holds the operation for a specific time period until the gate 2 completes its operation and Z_{out} is generated and fed to the input of Y_{out}, thus there is no delay mismatch and no chances of glitch occurrence. When the strobe signal is 0, it will not trigger the gate thus without strobe signal the circuit will not operate. Strobe has various advantages compared to other methods as it is easy to design and the code is re-usable such that the control used in a logic circuit can be implemented in any other circuit. It also reduces area and due to the lower circuit complexity it simulates faster and the power consumption and delay are very less. The major advantage is as the strobe signal uses only one control bit the gate of the one circuit will always wait for the other to finish so thus there will be no delay mismatch and moreover the control signal and the related codes are reusable and we need not design each and every time for separate circuits. Strobe signal has an added advantage compared to the DCDL structure as the DCDL structure uses combinational circuits and thus the power dissipation will be always more whereas the strobe signal uses sequential circuits and thus it won't consume more power.

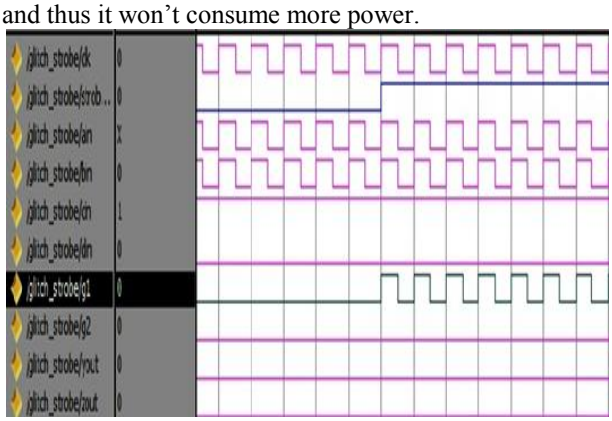

Fig.3 (b) Waveforms showing glitch free using strobe.

IV. DESIGN OF DIGITAL CONFIGURABLE ERROR FREE FREQUENCY DETECTOR USING STROBE SIGNAL.

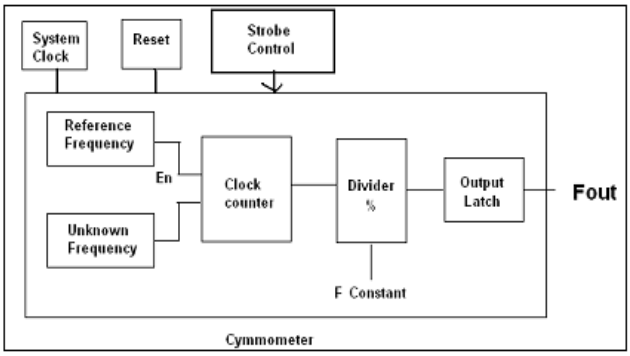

Fig.4 (a). configurable error free frequency detector

The structure shown in Fig. 4 shows a configurable error free frequency detector. configurable error free frequency detector is an electronic device used to measure frequency for a specified range. The frequency counter uses a reference frequency and an unknown frequency. The reference signal has to be specified as it provides the range and the unknown signal is the signal to be tested. Strobe control controls the operation of the gate for a specific period of time, so that there is no delay mismatch. It can control the occurrence of the glitch at both the rising edge and falling edge of the clock. The counter starts counting as soon as the strobe signal is 1 and the working of the circuit starts. Suppose the reference signal is 300 MHz, the counter will start counting as soon as the strobe signal is provided this can be clearly explained with the waveform.

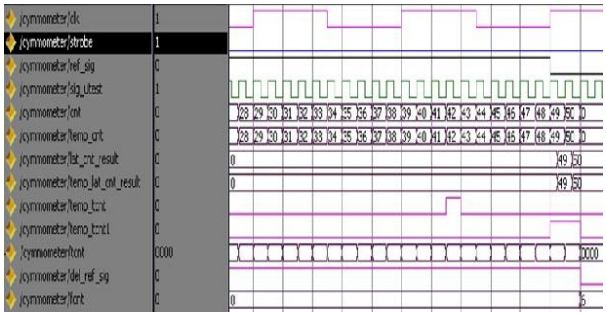

Fig.4 (b) waveform showing the strobe based configurable error free frequency detector.

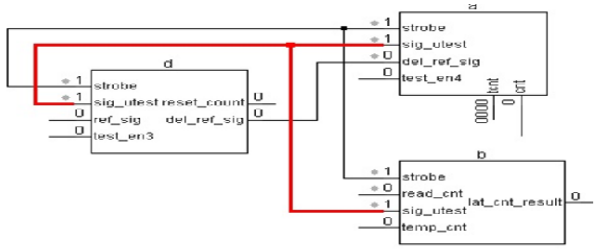

Fig. 4 (c) Dataflow diagram of the configurable error free frequency detector.

The data flow diagram clearly shows that when the strobe signal is 1the counter starts working. As the reference signal is provided as 300 MHz, the counter counts up to 50, and then again a new counter starts and likewise the counter generates 50 for 6 times. As the multiplier works for six times until the signal under test is generated. When the strobe signal is 1, it will trigger the gate and the operation starts and it will hold the operation for a specific period of time until the next gate completes its operation so that the output is generated at the same time and thus no delay mismatch and no occurrence of glitches. This concept not only removes the glitch but also makes sure that in further simulations glitches are not occurred, since the circuit will not operate when the strobe signal is 0,and the gate will not be triggered which in turn makes sure that the counter doesn't start counting. Moreover this concept is not only easy to design but also this code is reusable in any circuit using the strobe logic. The same control can be used in any platform as the strobe concept is mainly used nowadays to provide secure communications in WSN (Wireless Sensor Network), satellite communication, Frequency synthesizers and specially in DSP applications since FIFO (fast in fast out) is very prone to Glitching and thus by using the same concept of strobe we can control the occurrence of the glitches. The strobe logic provides a bulk of advantages over the NAND based DCDL concept as the DCDL utilizes combinational circuit the power dissipation is more compared to the sequential circuits which strobe control logic uses. Moreover it is easy to design and provides simple layout and also reduces area compared to the NAND based DCDL's. Strobe logic not only removes glitches but also makes sure that glitches are not produced any further and the same codes are reusable for any other application using strobe concept.

TABLE I. Comparison of all the glitch removing approaches

	Glitch	INL	Power dissipation	Design
Strobe based	no	0.8	0.77	Simple layout
NAND based	yes	0.7	0.92	complex
TINV based	no	0.6	1.49	complex
Mux based	no	0.3	1.33	simple

C. Applications of strobe controlled logic

The effectiveness of the proposed solution can be verified in many real time applications. The major applications are the [7] actively securing wireless communication like in WSN(Wireless Sensor Network), satellite communication, DSP applications like in GPS platform and also can be used in FIFO(Fast In Fast Out) as it is prone to high Glitching the strobe logic can be used, it can be also used in frequency synthesizers. In order to verify the effectiveness of the proposed solution in a real time application the configurable error free frequency detector has been redesigned by using proposed strobe control logic. The simulations confirm the correctness of the operation of strobe logic while

highlights the problems which arise when the NAND based DCDL is used in this application. The major drawback of NAND based DCDL is the increased delay, increased power dissipation and layout complexity.

V. CONCLUSION

A Strobe control module is presented which avoids the Glitching problem of previous circuits. A timing model of the Strobe structure implemented in the configurable error free frequency detector is developed to demonstrate the glitch free property of the proposed circuit. As an additional, the developed model also provides an explanation in order to guarantee a glitch free operation. The proposed Strobe signal logic can control the occurrence of glitch at both the rising and falling edge of the clock. The theoretical demonstration of the glitch free operation of the proposed Strobe signal module is also derived in the paper. Simulation results show that the correctness of the module with no delay mismatch compared to the previously proposed NAND based DCDL.

REFERENCES

[1] Davide De Caro, Senior member,*IEEE*, "Glitch free NAND based digitally controlled," *IEEE transactions on VLSI*, vol. 21,NO .1, January 2013.

[2] Arnold M. Frisch,"Self Calibrating strobe signal generator" *US Patent no US7219269*, May,2007.

[3] C.C Chung and C.Y.Lee*,"An all digital phase locked loop for high speed clock generation" IEEE j.Solid State Circuits*, vol. 38, no. 2, pp.347–351, Feb 2003.

[4] F. Lin, J. Miller, A. Schoenfeld, M. Ma, and R. J. Baker, "A register controlled symmetrical DLL for double-data-rate DRAM," *IEEE J.Solid-State Circuits*, vol. 34, no. 4, pp. 565–568, Apr. 1999

[5] R. J. Yang and S. I. Liu, "A 40–550 MHz harmonic-free all digital delay locked loop using a variable SAR algorithm," *IEEE J. Solid- State Circuits*, vol. 42, no. 2, pp. 361–373, Feb. 2007

[6] K. H. Choi, J. B. Shin, J. Y. Sim, and H. J. Park, "An interpolating digitally controlled oscillator for a wide range all digital PLL*," IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 2055–2063, Sep. 2009.

[7] Narendra Anand, Sung-Ju Lee, Edward W. Knightly,"Strobe:Actively securing wireless communications using zero forcing beam forming".